REMARKS

I. Introduction

Claims 2-8, 11, and 12 are pending in this application, of which claims 1, 11, and 12 are independent. All the claims stand rejected. Applicant submits that by the present Remarks, this application is placed in clear condition for immediate allowance.

II. The Rejection of Claims 2 and 11-12

Claims 2, 11, and 12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant Admitted Prior Art ("AAPA") in view of Gephardt et al. In the statement of the rejection, the Examiner admitted that the AAPA does not teach the non-transfer interval storing means. However, the Examiner asserted that Gephardt et al. teach the missing feature of the AAPA. The Examiner, then, concluded that it would have been obvious to modify the AAPA based on the teachings of Gephardt et al. to arrive at the claimed invention.

Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). The AAPA and Gephardt et al., either individually or in combination, do not teach a data transfer control system including all the limitations recited in claim 2. Specifically, the applied combination does not teach, among other things,

> transfer interval storing means for storing an interval between destination addresses of a plurality of one-word data which is included in the data which are to be transferred, the destination addresses being equally-separated with the interval; and
>
> bus cycle controlling means for controlling the data transfer such that, during a

> burst transfer, in a single bus cycle, a write control line of the bus is placed in a write-enabled state for a one-word data transfer period and is placed in a write-disabled state for an (N-1) words data transfer period periodically, wherein N is the number stored in the transfer interval storing means, and that data including a number of words which is equal to the number stored in the transferred-word number storing means is transferred while the write control line is in the write-enabled state.

Transfer Interval N

Claim 2 recites a transfer number (the number of words of data which are to be transferred), and a transfer interval N (N is the number stored in the transfer interval storing means). For example, if there are transfer destination addresses (1), (2), (3), (4), (5), (6), and (7) where the transfer number is 3 and the interval is 3, three pieces of data are transferred to the addresses (1), (4), and (7), as shown below

(1)	(2)	(3)	(4)	(5)	(6)	(7)
↑			↑			↑
Transfer			Transfer			Transfer

For example, according to the specification, when the value of transfer interval register 310 is set at 2 in Fig. 3A, control signal c_be#(303) becomes disabled (1111) at timing of T12 and enabled (00000) at timing of T13 to transfer one piece of data, as shown in Fig. 3B.

Gephardt et al. describe a direct memory access controller for performing a DMA transfer by executing both a memory access cycle and an I/O access cycle. However, Gephardt et al. is silent, at a minimum, on the claimed transfer interval N. The Examiner's cited portion (e.g., column 2, lines 52-65) simply describes disabling peripheral devices not involved in a DMA transfer. In fact, the Examiner did not specifically point out where Gephardt et al. describe the claimed transfer interval N. As admitted by the Examiner, the AAPA is also silent on the transfer interval N.

Accordingly, the applied combination of the AAPA and Gephardt et al. does not teach, at a minimum, "transfer interval storing means for storing an interval between destination addresses of a plurality of one-word data...," and "bus cycle controlling means for controlling the data transfer...," recited in claim 2.

Enabled period and disabled period

Applicant further submits that the AAPA and Gephardt et al. do not teach the claimed "one-word data transfer period" (enable period: e.g., B1 period) and the claimed "(N-1) words data transfer period" (disabled period: e.g., B2 period) with respect to N states of data transfer ("write-enable state" and "write-disable state" in claim 1). In claim 1, the write control line is placed in the write-enabled state in the "one-word data transfer period" (B1 period) and is placed in the write-disable state in the "one-word data transfer period" (B2 period), so that one piece of data is transferred during these periods (B period (B1 + B2)). For example, it may be said that controls signals are enabled in the B1 period and disabled in the B2 period, and one piece of data is transferred during the B period.

On the other hand, Gephardt et al. do not teach any distinction between the alleged "one-word data transfer period" (B1 period) and the "one-word data transfer period" (B2 period), as claimed. The reference simply teaches that control signals for a DMA transfer device are enabled and those for other devices are disabled throughout the same period (B period) of performing a DMA transfer (see column 2, lines 52-65). In other words, control signals related to DMA transfer are not disabled in Gephardt et al. Accordingly, it is submitted that Gephardt et al. do not teach the claimed bus cycle controlling means.

Thus, the AAPA and Gephardt et al., either individually or in combination, do not teach a data transfer control system including all the limitations recited in independent claim 2. The

above discussion is applicable to independent claims 11 and 12. Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 2, 11 and 12.

III. The Rejection of Dependent Claims 3-8

Claims 3 and 7 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA and Gephardt et al. and further in view of Sheafor et al. and Kreifels; claim 4 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA and Gephardt et al. and further in view of Fabre; claim 5 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA, Gephardt et al., and Sheafor et al., and further in view of Kreifels and Fabre; claim 6 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA and Gephardt et al. and further in view of Kreifels; and claim 8 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA, Gephardt et al., and Fabre, and further in view of Kreifels.

Each of the above rejections of claims 3-8 is traversed. Specifically, claims 3-8 depend from independent claim 2. Applicant incorporates herein the arguments previously advanced in traversing the imposed rejection of claim 2 under 35 U.S.C. § 103 for obviousness predicated upon the AAPA in view of Gephardt et al. The Examiner's additional comments and secondary references to Sheafor et al., Kreifels, and Fabre do not cure the previously argued deficiencies in the attempted combination of the AAPA and Gephardt et al.

Applicant, therefore, submits that the imposed rejection of claims 3-8 under 35 U.S.C. §103 are not factually or legally viable and, hence, respectfully solicits withdrawal thereof.

Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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